## REMARKS

This responds to the Office Action mailed on January 11, 2005.

Claims 1 and 11 are amended, no claims are canceled, and no claims are added; as a result, claims 1-45 are now pending in this application, of which claims 26-35 and 42-45 are withdrawn from consideration. Thus, claims 1-25 and 36-41 are under examination.

### *§102 Rejection of the Claims*

Claims 1-5 and 11-14 were rejected under 35 USC § 102(b) as being anticipated by Hammond et al. (U.S. 2003/0013323 A1). Applicant respectfully traverses this rejection.

The cited reference of Hammond discloses forming both buried channel devices and surface channel devices on a hetero-structure substrate and *horizontally* isolating the devices by selectively removing silicon germanium alloys in the form of *vertical* isolation trenches 34, 36 and 38. There is no separate vertical isolation other than the inherent electrical reverse bias of the various diodes 40 and 42 that form portions of the electrical devices.

Applicant respectfully submits that the Office Action is incorrect in stating, on page 2, that "Hammond et al discloses vertically isolating the strained silicon layer 20 from the substrate 12 by undercutting with isolation SiGe regions 32, which undercut and extend partially under strained silicon layer 20, as shown in Figure 5, and as disclosed in Paragraph 0024". Applicant submits that there is nothing in the cited portion of the reference that discusses vertical isolation, and that the partial undercut shown in figure 5 is so slight as to be insignificant.

Nevertheless, Applicant has amended independent claims 1 and 11 to make the difference between the present subject matter and the cited reference more explicit. Specifically, independent claim 1, as recited herein, recites "*...vertically isolating the strained silicon layer from the substrate by undercutting the semiconductive silicon compound layer and filling the entire area under the semiconductive compound with an electrical insulator ...*", which combination of features is not found in the cited reference of Hammond. The cited reference has only semiconductor layers below the devices, specifically the strained silicon layers 20 and 16, the SiGe layers 18 and 14, and the silicon substrate 12. There is no suggestion of an insulator layer below the semiconductor layers, as found in the present subject matter.

Independent claim 11 is clearly distinct over the cited reference of Hammond at least because claim 11, as amended herein, recites "*...vertically isolating the strained silicon layer from the substrate by undercutting the relaxed layer and filling the entire area under the relaxed layer with an electrical insulator ...*", which combination of features is not found in the cited reference of Hammond. As noted above with reference to the rejection of claim 1, there is no suggestion in Hammond of an insulator layer below the semiconductor layers, as is found in the present subject matter.

The dependent claims 2-5 and 12-14 are seen as being patentable at least as depending from base claims shown above to be patentable. In light of the above-described claim amendments, Applicant respectfully requests that this rejection be reconsidered and withdrawn.

*Allowable Subject Matter*

Claims 6-10, 15-25, and 36-41 were allowed. Applicant thanks the Examiner for the indication of allowable subject matter.

## CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney David Suhl at 508-865-8211, or the below-signed attorney at (612) 373-6960, to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

LEONARD FORBES

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Date 3-11-05

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop AF, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 11 day of March, 2005.

KACIA LEE _____
Name

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